

REMARKS

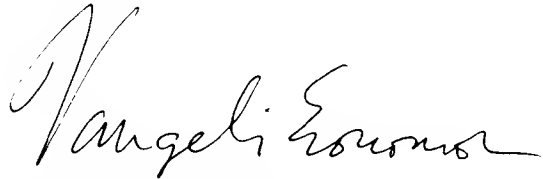
Reconsideration is respectfully requested.

The Office Action dated December 27, 2002 indicates that Claims 1-9 are rejected for lack of essential elements. Claims 1 and 5 have been amended to provide the structural connection required, and Claims 2, 7 and 9 have been amended to overcome the other noted inconsistencies.

The Office Action further indicates that Claims 1-9 would be allowable over the prior art of record in the event that the §112 rejection is overcome, for which indication the Applicants express their appreciation.

It is respectfully submitted that the above amendments have overcome the outstanding rejections. Accordingly, a Notice of Allowance is earnestly solicited.

Respectfully submitted,



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MARKED UP COPY OF THE CLAIMS

1. (Amended) A fringe field switching mode liquid crystal display, comprising:
 - gate lines and data lines aligned on a transparent insulating substrate to vertically cross each other;
 - common electrode lines aligned horizontally to the gate lines;
 - a pixel region defined in a space formed by the gate lines and data lines;
 - a first transparent electrode formed in the pixel region, and divided into at least two regions; and
 - a second transparent electrode insulated from the first transparent electrode, and divided [on] in the second [first] transparent electrode into as many regions as in the first transparent electrode, a data voltage being applied to the second transparent electrode in a first region and to the first transparent electrode in a second region via a common electrical connection, [a] the sum of the voltages applied to the pixel region having a zero voltage.
2. (Amended) The device according to claim 1, wherein the first transparent electrode formed in the first region and the second transparent electrode formed in the second region are connected to a common electrode line to provide the common electrical connection.
5. (Amended) A method for fabricating a fringe field switching mode liquid crystal display having gate lines and data lines aligned on a transparent insulating substrate to vertically cross each other, common electrode lines aligned horizontally to the gate lines, a thin film transistor formed by a source and drain extended from the data line, and the gate line, and a pixel region defined in a space formed by the gate lines and data lines, comprising the steps of:

forming a first transparent electrode in the pixel region to be divided into at least two regions; and

forming a second transparent electrode to be insulated from the first transparent electrode and divided [on] in the [first] second transparent electrode into as many regions as in the first transparent electrode, such that when a data voltage [being] is applied to the second transparent electrode in a first region and to the first transparent electrode in a second region via a common electrical connection, [a] the sum of the voltages applied to the pixel region [having] have a zero voltage.

7. (Amended) The method according to claim 6, further comprising the steps of:

forming an insulating film over the [resultant] structure resulting from the steps of Claims 5 and 6 including the first transparent electrode divided into at least two regions, and forming a contact hole on the insulating film to expose the first transparent electrode portion of the second region; and

forming a second transparent electrode layer on the insulating film having the contact hole, and forming a second transparent electrode divided into two regions by patterning the second transparent electrode layer.

9. (Amended) The [device] method according to claim 5, wherein the first transparent electrode is formed in a box shape, and the second transparent electrode is formed in a slit shape to apply an electric field to a liquid crystal.